

IN THE SPECIFICATION:

Please replace the paragraph beginning at line 24 of page 1 with the following rewritten paragraph:

-- One of the rendering methods is polygon rendering. In this method, a three-dimensional model is expressed as a composite of triangular unit graphics (polygons). By drawing the polygons as units, the colors of the pixels of the display screen are decided. --

Please replace the paragraph beginning at line 17 of page 26 with the following rewritten paragraph:

-- The operation sub-blocks 203₁ to 203₈ perform the above blending and output the (R, G, B, α) data S203₁ to S203₈ only when results of the level detection of the val data S220₁ to S220₈ by the clock enablers 213₁ to 213₈ are "1." --

Please replace the paragraph beginning at line 23 of page 26 with the following rewritten paragraph:

-- The operation block 204 has the operation sub-blocks 204₁ to 204₈ and performs a z-comparison for the input (R, G, B, α) data S203₁ to S203₈ by using the content of the z-data stored in the z-buffer 22. When the image drawn by the (R, G, B, α) data S203₁ to S203₈ is positioned closer to the viewing point than the image drawn in the display buffer 21 the previous time, the operation block 204 updates the z-buffer 22 and

outputs the (R, G, B, α) data S203₁ to S203₈ as the (R, G, B, α) data S204₁ to S204₈ to the operation sub-blocks 205₁ to 205₈ of the operation block 205. --

Please replace the paragraph beginning at line 15 of page 27 with the following rewritten paragraph:

-- The operation block 205 has the operation sub-blocks 205₁ to 205₈, blends the (R, G, B, α) of the data S204₁ to S204₈ and the (R, G, B) data already stored in the display buffer 21 by the blending ratio indicated in the α data included in the (R, G, B, α) data S204₁ to S204₈, and writes the blended (R, G, B) data S205₁ to S205₈ in the display buffer. --

Please replace the paragraph beginning at line 25 of page 29 with the following rewritten paragraph:

-- Here, a case of, for example, simultaneous processing on 8 pixels in a block 31 shown in Fig. 12 will be considered. In this case, the val data S220₁, S220₂, S220₃, S220₅, and S220₆ indicate "0" and the val data S220₄, S220₇, and S220₈ indicate "1." --

Please replace the paragraph beginning at line 8 of page 30 with the following rewritten paragraph:

-- Then in the clock enablers 210₁ to 210₈, the levels of the respective val data

S220₁ to S220₈ are detected. Specifically, "1" is detected in the clock enablers 210₄, 210₇, and 210₈ and "0" is detected in the clock enablers 210₁, 210₂, 210₃, 210₅, and 210₆. --

Please replace the paragraph beginning at line 25 of page 30 with the following rewritten paragraph:

b7
-- Next, the clock enablers 211₁ to 211₈ of the operation sub-blocks 201₁ to 201₈ detect the levels of the respective val data S220₁ to S220₈. --

Please replace the paragraph beginning at line 10 of page 31 with the following rewritten paragraph:

b8
-- On the other hand, no operation is performed in the operation sub-blocks 201₁, 201₂, 201₃, 201₅, and 201₆. --

Please replace the paragraph beginning at line 8 of page 32 with the following rewritten paragraph:

b9
-- Next, the clock enablers 213₁ to 213₈ of the operation sub-blocks 203₁ to 203₈ detect the levels of the respective val data S220₁ to S220₈. --

Please replace the paragraph beginning at line 11 of page 32 with the following rewritten paragraph:

b10
-- Then, based on the detection results, only the operation sub-blocks 203₄, 203₇,

b10 and 203₈ blend the texture data (R, G, B, α) S202₄, S202₇, and S202₈ input from the operation block 202 and the (R, G, B) data included in the DDA data S11 from the triangle DDA circuit 11 by the blending ratio indicated by the α data (texture α) included in the (R, G, B, α) data S202₄, S202₇, and S202₈ to generate the blended data (R, G, B). --

Please replace the paragraph beginning at line 14 of page 36 with the following rewritten paragraph:

b11 -- Here, the DDA set-up circuit 10, the texture engine circuit 12, the CRT controller circuit 14, the RAMDAC circuit 15, the DRAM 16, and the SRAM 17 are the same as those explained in the first embodiment. --

Please replace the paragraph beginning at line 6 of page 44 with the following rewritten paragraph:

b12 -- The operation block 500 has operation sub-blocks 501₁ to 500₈ and receives as input the DDA data S11 from the triangle DDA circuit 11 shown in Fig. 7. --

Please replace the paragraph beginning at line 9 of page 44 with the following rewritten paragraph:

b13 -- The operation sub-blocks 501₁ to 500₈ detect the levels of the val data S220₁ to S220₈ included in the DDA data S11 in the respective clock enablers 510₁ to 510₈ and

B13
perform the z-comparison when the level is "1" (when the pixel is inside a triangle being processed), while do not perform the z-comparison when the level is not "1." --

Please replace the paragraph beginning at line 6 of page 47 with the following rewritten paragraph:

B14
-- The operation block 503 has operation sub-blocks 503₁ to 503₈, outputs a read request including the texture coordinate data (u, v) generated in the operation block 502 to the SRAM 17 or DRAM 16 via the memory I/F circuit 13, and reads the texture data stored in the SRAM 17 or the texture buffer 20 via the memory I/F circuit 513 to obtain the (R, G, B, α) data S17 stored in the texture address corresponding to the (u, v) data. --

Please replace the paragraph beginning at line 7 of page 49 with the following rewritten paragraph:

B15
-- First, the clock enablers 510₁ to 510₈ of the operation sub-blocks 500₁ to 500₈ detect the levels of the val data S220₁ to S220₈ included in the DDA data S11. When the detected level is "1" (when the pixel is inside the triangle being processed), the z-comparison is performed. --

Please replace the paragraph beginning at line 2 of page 52 with the following rewritten paragraph:

-- Next, in the clock enablers 515₁ to 515₈ of the operation sub-blocks 505, to

b16
505₈, the levels of the val data S220₁ to S220₈ and S500a₁ to S500a₈ are detected. Only when both of the levels are "1," the (R, G, B, α) data S504₁ to S504₈ and the (R, G, B) data already stored in the display buffer 21 are blended by the blending ratio indicated by the α data included in the respective (R, G, B, α) data S504₁ to S504₈. The blended (R, G, B) data S505₁ to S505₈ are written in the display buffer 21. --

Please replace the paragraph beginning at line 5 of page 53 with the following rewritten paragraph:

b17
-- For example, in the above second embodiment, as shown in Fig. 6, an example was given of the case where 8 pixels of data were simultaneously processed in the operation blocks of the texture engine circuit 12 and the memory I/F circuit 413. However, as shown in Fig. 9, 1 pixel of data may be processed in the operation blocks as well. --

Please replace the paragraph beginning at line 18 of page 53 with the following rewritten paragraph:

b18
-- Also, in the above third embodiment, as shown in Fig. 8, an example was given of the case where 8 pixels of data were simultaneously processed in the operation blocks of the texture engine circuit 512 and the memory I/F circuit 513. However, as shown in